Integrated Circuit Design
ELCT 701
(Winter 2019)
Lecture 1: Introduction

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Course Overview

Course Team

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<thead>
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<td>Office hours: Via E-mail</td>
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<table>
<thead>
<tr>
<th>Teaching Assistant</th>
<th>Eng.: Sandy Atef</th>
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<td>Office hours: Via E-mail</td>
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Teaching Method

<table>
<thead>
<tr>
<th>Teaching Method</th>
<th>Location</th>
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<tbody>
<tr>
<td>One Lecture per Week (Wednesday 1st Slot)</td>
<td>H9</td>
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<tr>
<td>One Tutorial per Week (Tuesday 1st/3rd)</td>
<td>Check Your Schedule</td>
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Evaluation Method

<table>
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<tr>
<th>Evaluation Method</th>
<th>Percentage %</th>
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<tr>
<td>Assignments</td>
<td>10</td>
</tr>
<tr>
<td>Quizzes</td>
<td>15</td>
</tr>
<tr>
<td>Mid-Term</td>
<td>30</td>
</tr>
<tr>
<td>Final</td>
<td>45</td>
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Course Guidelines

- Please follow GUC regulations for attendance

Course Prerequisites:
- Semiconductors
- Electronic Circuits
- Electric Circuits I and II
- Digital System Design

Course Objectives:
- Design and analyze digital circuits on transistor level
- Define different design alternatives in studying Dynamic Logic Circuits to build high performance digital integrated circuits
- Discuss different types of digital memories
# Tentative Course Schedule

<table>
<thead>
<tr>
<th>Lecture #</th>
<th>Topic</th>
<th>Description</th>
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<tbody>
<tr>
<td>1</td>
<td>Introduction to Integrated Circuit Design</td>
<td>Historical Background on IC Industry</td>
</tr>
<tr>
<td>2</td>
<td>Revision on Semi-Conductor Devices and their electrical modeling</td>
<td>PN Junctions, Transistors I-V modeling</td>
</tr>
<tr>
<td>3</td>
<td>MOS Inverter: Static Behavior</td>
<td>Transistor Level Implementation of Inverters (Large Signal Analysis)</td>
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<tr>
<td>4</td>
<td>CMOS Inverter: Dynamic Behavior</td>
<td>Transistor Level Implementation of Inverters (Transient Analysis)</td>
</tr>
<tr>
<td>5</td>
<td>Interconnect and Delay</td>
<td>Delay introduced by wiring interconnect</td>
</tr>
<tr>
<td>6</td>
<td>Inverter: Power Consumption Calculations</td>
<td>Static and Dynamic Power Consumption Calculations</td>
</tr>
<tr>
<td>7</td>
<td>Design of Combinational Logic Circuits (Static &amp; Dynamic)</td>
<td>Transistor Level Implementation of NOR, NAND and XOR Gates (Transistor Level)</td>
</tr>
<tr>
<td>8</td>
<td>Design of Sequential Logic Circuits (Static &amp; Dynamic)</td>
<td>Transistor Level Implementation of Latches, Flip-flops and Registers</td>
</tr>
<tr>
<td>9</td>
<td>Arithmetic Building Blocks</td>
<td>Transistor Level Implementation of Adder, Multiplier and Shifter</td>
</tr>
<tr>
<td>10 &amp; 11</td>
<td>Design of Memory and Array Structures</td>
<td>Transistor Level Implementation of SRAM, DRAM, ROM transistor level</td>
</tr>
<tr>
<td>12</td>
<td>Timing Analysis for Digital IC Circuits</td>
<td>Timing Constraints</td>
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# Tentative Assessment Schedule

<table>
<thead>
<tr>
<th>Week #</th>
<th>Quizzes</th>
<th>Assignments</th>
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<tbody>
<tr>
<td>4</td>
<td><strong>Quiz 1</strong>: Devices modeling and Inverter DC Characteristics</td>
<td><strong>Assign. 1</strong>: Layout of different Inverters and their DC Characteristics analysis</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td><strong>Assign. 2</strong>: Static MOS Combinational Logic</td>
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<tr>
<td>7</td>
<td><strong>Quiz 2</strong>: Dynamic Combinational logic</td>
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<tr>
<td>8</td>
<td></td>
<td><strong>Assign. 3</strong>: Static &amp; Dynamic Sequential Logic</td>
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<tr>
<td>9</td>
<td><strong>Quiz 3</strong>: Sequential logic</td>
<td></td>
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<tr>
<td>11</td>
<td><strong>Quiz 4</strong>: Memories</td>
<td><strong>Assign. 4</strong>: Digital IC Building blocks</td>
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Course Grading Rules

- Grading scheme is based on GUC Regulations
- Copies will be graded as **ZERO**
  - This is applicable for Assignments
- Stick to the office hours for questions
- Send an e-mail for urgent questions
- Attend the lectures and take notes!
- All the Course material will be available on the website
References

   Rabaey, Chanderakasan and Nikolic


3. “CMOS VLSI Design: A Circuits and Systems Perspective”, Neil H. E. Weste and David Money Harris
IC Design History and Present

Overview
IC History

- First Transistor was introduced in 1947 at Bell Labs, Point Contact Transistor
- First BJT in 1949 by Schockley
- BJT based logic gate made by discrete components was introduced in 1956 by Harris
- Integrated Circuit concept was introduced through Texas Instruments by Jack Kilby (Nobel Prize Winner)
First functioning Silicon planar IC chip (All components on a single Silicon crystal) was made by R. Noyce of Fairchild Camera in 1961.

It was a flip-flop circuit containing **Six** devices.
IC History

- MOS transistor principle was introduced in 1925 by J. Lilienfeld.
- In 1959, Dawon Kahng and Martin M. Atalla at Bell labs invented the MOS.
- In 1963 C. T. Sah and Frank Wanlass of the Fairchild R & D Laboratory showed that logic circuits combining p-channel and n-channel MOS transistors in a complementary symmetry circuit configuration drew close to zero power in standby mode.
- Wanlass patented the idea that today is called CMOS.
ASIC vs. Discrete Electronics

Discrete Electronics Ex.: Microphone Circuit
ASIC vs. Discrete Electronics

Wireless transceiver IC (Infineon Company)

Example of IC: Wireless transceiver Block Diagram
## ASIC vs. Discrete Electronics

<table>
<thead>
<tr>
<th>Specification</th>
<th>Discrete Electronics</th>
<th>ASICs</th>
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<tbody>
<tr>
<td><strong>Area</strong></td>
<td>Large</td>
<td>Small</td>
</tr>
<tr>
<td><strong>Functionality</strong></td>
<td>Dedicated to a Specific Part of the system</td>
<td>Complete systems exist on a small Chip</td>
</tr>
<tr>
<td><strong>Configurability</strong></td>
<td>Easy</td>
<td>Complex</td>
</tr>
<tr>
<td><strong>Price</strong></td>
<td>Cheap</td>
<td>Expensive</td>
</tr>
<tr>
<td><strong>Application</strong></td>
<td>Small Production</td>
<td>Mass Production (Cost decreases!)</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td><strong>Design parameter</strong></td>
<td>Discrete elements</td>
<td>Transistor sizing or external biasing voltage/current</td>
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</table>
The observation made in 1965 by Gordon Moore, co-founder of Intel, that the number of transistors per square inch on integrated circuits had doubled every year since the integrated circuit was invented.
IC Present Day

- "Core i7" processor is of a size slightly greater than a coin
- Operates with a clock frequency 3.4GHz
- Minimum channel length of transistor (2*32nm)
- Power: 130W with maximum supply of 1.4V
- No. of transistors on Chip: 1,400,000,000

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IC Present Day

- How can the design engineers integrate such a large number of transistors on one chip (Design level for Digital electronics)?
  - Using Divide and conquer
  - Abstraction can be done on Digital Circuits successfully
  - Designer focus on optimizing a standard cell and reuse it (CAD Tools are used)

- IC Design Course focus on the three intermediate steps
  - Device (Transistor)
  - Circuit (inverter)
  - Gate
  - Module (Ex.: adder)
  - System
How can the design engineers integrate such a large number of transistors on one chip (Design level) when dealing with analog Circuits?

- Abstraction can not be done in Analog world easily (Transistor sizing changes everything in the circuit)
- Microelectronics Course will focus on the analog design part
IC Design Flow

- Integrated Circuit Design Flow chart:
  - Our course main objective is to study how to design basic digital circuits used in ICs
  - Examples: inverters, Gates, Flip-flops
  - Circuit design is done in our course on Transistor level and layout level
  - Integrated circuit Course and VLSI courses are dedicated to Digital electronics and physical design of the ICs
  - At the end of the course, the student can design basic Digital IC building blocks on the circuit level and on the physical level.

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What happens when a new Technology is launched to the market?

First Step: Fabrication (FAB) companies (Ex. TSMC) provides a new technology where the MOS Channel length can be decreased

- Smaller transistor means more devices can be integrated on one chip
- MOS can operate at lower voltage supplies (gate oxide thickness is decreased as well)
- Now we reached 28nm (minimum channel length is twice this no.), they call it λ

Second Step: the FAB provide the circuit level designers with a model for the transistor

- Process parameters (Threshold voltage calculations, transconductance gain, parasitic capacitances, etc.)
IC Design Flow

- What happens when a new Technology is launched to the market? (Cont.)

  - **Third Step:** Circuit level designer tries to build a basic circuit with the new tech. and creates a model for it
    - Designers push the new tech. to its maximum limit to get the best performance possible (less area, power and high speed)
    - The basic circuit could be an inverter, gate or module depending on the target End product

  - **Fourth Step:** layout engineers start to make the physical circuit corresponding to the basic circuit designed in previous step
    - They draw the geometries of the drains, sources and gates of the transistor
    - Also they plan the contacts and connections between the transistors in the circuit
    - This is done using different layers of materials (Semi. Tech. Course!)
IC Design Flow

- What happens when a new Technology is launched to the market? (Cont.)
  - **Fifth Step:** Layout Engineers must follow the FAB Design rules (DRC)
    - The Design rules determine the minimum length the FAB can control on the wafer
    - They also define the spaces between same layers and interconnection layers
      - What is the separating distance between two transistors sources or gates?
      - What is the separating distance between two layers (gate and drain of same transistor)
  - **Sixth Step:** Layout Engineers check their layout versus the circuit design (LVS)
  - **Final Step:** Fabrication and Testing (Measurements)
Digital Circuits Design

Performance Metrics
Digital Circuit Design Concerns

- Digital Electronic circuits must fulfill the following requirements:
  - **Cost** (The less the better)
  - **Area** (The less the better)
  - **Functionality** (Circuit is operating correctly)
  - **Robustness** (What is the effect of Process Variations during fabrication on the circuit)
  - **Performance** (How fast the circuit will work?)
  - **Power and Energy Consumption** (The less the better)

- In our course we will focus on how to calculate these performance metrics for Digital circuits!
Appendix

Fabrication process of CMOS Inverter
CMOS Inverter

<table>
<thead>
<tr>
<th>A</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
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</tbody>
</table>
CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process
- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors
Well and Substrate Taps

- Substrate must be tied to GND and n-well to $V_{DD}$
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps

Substrate tap

Well tap

p substrate

n well

GND

$V_{DD}$

n++
p++

n++
p++

A

Y
Transistors and wires are defined by masks

Cross-section taken along dashed line

Inverter Mask Set
Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal
Fabrication

- Chips are built in huge factories called FABs
- Contain clean rooms as large as football fields
Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO$_2$ (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO$_2$
Oxidation

- Grow SiO$_2$ on top of Si wafer
  - 900 – 1200 °C with H$_2$O or O$_2$ in oxidation furnace

Diagram:

```
  p substrate
  SiO$_2$
```
Spin on photoresist
- Photoresist is a light-sensitive organic polymer
- Softens/hardens where exposed to light
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist
Etch

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed

```
| p substrate | SiO₂ | Photoresist |
```

```
Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn’t melt in next step
n-well

- n-well is formed with diffusion or ion implantation
- **Diffusion**
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- **Ion Implantation**
  - Blast wafer with beam of As ions
  - Ions blocked by SiO$_2$, only enter exposed Si

![Diagram of n-well and SiO$_2$]
Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps
Polysilicon

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH₄)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor
Use same lithography process to pattern polysilicon
Self-Aligned Process

- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact

Diagram:
- p substrate
- n well
N-diffusion

- Pattern oxide and form n+ regions
- Self-aligned process where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn’t melt during later processing
Historically dopants were diffused
Usually ion implantation today
But regions are still called diffusion
Strip off oxide to complete patterning step
Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact.
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed
Metalization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires

Diagram:
- p substrate
- n well
- Metal
- Thick field oxide

Legend:
- p+
Layout

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size $f = \text{distance between source and drain}$
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f / 2$
  - E.g. $\lambda = 0.3 \ \mu m$ in 0.6 $\mu m$ process
Simplified Design Rules

- Conservative rules to get you started

Diagram showing:
- Metal1 spacing and width
- Metal2 spacing and width
- Diffusion and Polysilicon layers
- Metal1-Diffusion, Metal1-Polysilicon, Metal1-Metal2 contact and via rules
Inverter Layout

- Transistor dimensions specified as Width / Length
  - Minimum size is $4\lambda / 2\lambda$, sometimes called 1 unit
  - In $f = 0.6 \, \mu m$ process, this is $1.2 \, \mu m$ wide, $0.6 \, \mu m$ long
Summary

- MOS transistors are stacks of gate, oxide, silicon
- Act as electrically controlled switches
- Build logic gates out of switches
- Draw masks to specify layout of transistors

- Now you know everything necessary to start designing schematics and layout for a simple chip!
About these Notes

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IC Design Flow

https://www.youtube.com/watch?v=bor0qLifjz4