Memories


- Memory arrays capable of storing large quantities of digital information are essential to all digital systems.
- The keys for memory design criteria are:
  1. Area: number of bits stored per unit area
  2. Speed: i.e. the time required to access the memory either to read or store a particular data bit
  3. Static/ dynamic Power
- Memories are classified according to the type of data storage and data access.
  The RAM (Random Access Memory) is the type of our concern which is the read/write memory.

- Based on the operation type of the data storage cells, RAMs are classified into:
  1. Dynamic RAM (DRAM):
     - Consists of a capacitor to store the information bit and a transistor to access the capacitor. Since DRAMs, as any dynamic circuit, depends on charge storage on a capacitor, therefore DRAMs need a periodic operation (refreshing: reading and rewriting periodically), since the cell information is degraded due to leakage current at the storage node.
     - DRAM is widely in main memory used due to its low cost and high density.
  2. Static RAM (SRAM):
     - Consists of a latch and therefore data is kept as long as power is ON and refreshing is not required.
     - SRAMs are mainly used for cache memory due to its high speed and low power consumption
Prob.1: A single-transistor DRAM cell is represented by the following circuit diagram (Fig. 10.1). The bit line can be pre-charged to \(V_{DD}/2\) by using a clocked pre-charge circuit. Also the WRITE circuit is assumed here to bring the potential of the bit line to \(V_{DD}\) or \(0V\) during the WRITE operation with word line at \(V_{DD}\). Using the parameters given:

- \(V_{To} = 1\ V\)
- \(\gamma = 0.3\ V^{0.5}\)
- \(|2\Phi_F| = 0.6\ V\)

![Diagram showing DRAM cell with precharge and write circuits.](image)

*Fig. 10.1\(^1\)*

a. Find the maximum voltage across the storage capacitor \(C_s\) after WRITE-1 operation, i.e., when the bit line is driven to \(V_{DD} = 5\ V\).
b. Assuming zero leakage current in the circuit, find the voltage at the bit line during READ-1 operation after the bit line is first pre-charged to \(V_{DD}/2\).
**General explanation of the circuit:**

- The above circuit represents a single cell in a dynamic RAM, where each cell is responsible of one bit.
- The capacitor $C_s$ is an explicit capacitor - and not the parasitic capacitances. $C_s$ is responsible of storing the data bit by storage of the corresponding charge on its node.
- The capacitor $C_{BL}$ represents all the parasitic capacitances seen at this bit line which is connected to a whole column of similar cells.
- To access the cell for either a read or write, it must be enabled through the gate of the MOS transistor by enabling the word line to $V_{DD}$.

- **During a write operation:**
  - To write a logic ‘1’ inside the cell, the write circuitry gives the bit line a logic ‘1’ i.e. voltage = $V_{DD}$. Therefore the capacitance $C_{BL}$ will discharge in the storage capacitance $C_s$ building a logic ‘1’ in the cell.
  - To write a logic ‘0’ inside the cell, the write circuitry gives the bit line a logic ‘0’ i.e. voltage = 0. Therefore the capacitance $C_s$ will discharge in the bit line capacitance $C_{BL}$ building a logic ‘0’ in the cell.

- **During a read operation:**
  To read any value inside the cell is, the bit line is given a voltage of $V_{DD}/2$
  - If the cell is holding a logic ‘0’, i.e. voltage = 0, therefore the capacitance $C_{BL}$ will discharge in the storage capacitance $C_s$ causing the voltage on the bit line to decrease less than $V_{DD}/2$ signaling that this is a read “0” operation.
  - If the cell is holding a logic ‘1’, i.e. voltage = $V_{DD}$, therefore the capacitance $C_s$ will discharge in the bit line capacitance $C_{BL}$ causing the voltage on the bit line to increase more than $V_{DD}/2$ signaling that this is a read “1” operation.

- **Note:**
  Given 2 capacitors $C_1$ and $C_2$ connected together through a switch, when the switch is closed i.e. both capacitors are connected, if voltage on $C_1$ is higher than voltage on $C_2$, therefore a current flows from $C_1$ to $C_2$, causing $C_1$ to lose some of its charge while building extra charge on $C_2$; which means that as long as the current is flowing voltage on $C_1$ decreases and voltage on $C_2$ increases till the point where the current stops.
  The aim is always to find when the current will stop to know the final voltage on each capacitor.
**Solution:**

a) To write a ‘1’ in the cell initially:
- Bit line is driven to $V_{DD} = 5\, V$,
- The gate of the MOS transistor is driven to $V_{DD} = 5\, V$ to enable the access of the cell
- The cell holds initially a zero, i.e. Voltage on $C_S = 0$

- Current will flow as shown in the above circuit, and voltage on $C_S$ will increase and on $C_{BL}$ will decrease till the current stops.
- **The current will keep flowing as long as 2 conditions are valid:**
  1. $V_{GS} \geq V_T$
     - i.e. $V_G - V_S \geq V_T$
     - $5 - V_S \geq 1$
     - $V_S \text{ max} \geq 5 - 1 = 4\, \text{Volts}$
     - $V_S$ is the voltage on $C_S$ which is increasing, and according to the first condition it can reach a maximum of only 4 Volts
  2. $V_{on\, C_{BL}} \neq V_{on\, C_S}$
     - Since if both voltages are equal no more charge is transferred from on capacitor to the other which means no more current flows.
     - According to the charge sharing/transfer rule, charge will keep transferring till both voltages are equal:
     - Charge lost by $C_{BL} = \text{charge gained by } C_S$
     - $\Delta Q_{C_{BL}} = \Delta Q_{C_S}$
     - $C_{BL}\Delta V_{C_{BL}} = C_S\Delta V_{C_S}$
     - $C_{BL}(V_{C_{BL}\text{ initial}} - V_{final}) = C_S(V_{final} - V_{C_S\text{ initial}})$
     - $450(5 - V_{final}) = 50(V_{final} - 0)$
     - $V_{final} = 4.5\, \text{volts}$
Since Voltage on $C_S$ is increasing, therefore it can only reach the 4 volts, then the current will not flow any more since the 1st condition will be violated and therefore it will never reach the 2nd condition.

b) To read a ‘1’ already stored in the cell, the initial values are:

- bit line is driven to $\frac{V_{DD}}{2} = 2.5 \text{ V}$,
- The gate of the MOS transistor is driven to $V_{DD} = 5 \text{ V}$ to enable the access of the cell
- The cell holds a ‘1’, i.e. Voltage on $C_S = 4 \text{ volts}$ (since this is the maximum reached voltage when we wrote a ‘1’ in the cell)

- Checking both conditions:
  1. $V_{GS} \geq V_T$
     
     i.e. $V_G - V_S \geq V_T$
     
     $5 - V_S \geq 1$
     
     $V_S \text{ max} \geq 5 - 1 = 4 \text{ Volts}$
     
     $V_S$ is the voltage on $C_{BL}$ which is increasing, and according to the first condition it can reach a maximum of only 4 Volts

  2. $V_{on\ C_{BL}} \neq V_{on\ C_S}$

     Charge lost by $C_{BL} = \text{charge gained by } C_S$
     
     $\Delta Q_{C_{BL}} = \Delta Q_{C_S}$
     
     $C_{BL} \Delta V_{C_{BL}} = C_S \Delta V_{C_S}$
     
     $C_{BL}(V_{final} - V_{C_{BL initial}}) = C_S(V_{C_S initial} - V_{final})$
     
     $450(V_{final} - 2.5) = 50(5 - V_{final})$
     
     $V_{final} = 2.65 \text{ volts}$
     
     Since Voltage on $C_{BL}$ is increasing, therefore it can only reach the 2.65 volts, then the current will not flow any more since the 2nd condition will be violated and therefore it will never reach the 1st condition.
Prob.2: Consider the SRAM cell shown in Fig. 10.2. Transistors $M1$ and $M2$ have $(W/L)$ values of $4/4$. Transistors $M3$ and $M4$ have $(W/L)$ values of $2/4$. $M5$ and $M6$ are to be sized such that the state of the cell can be changed for $V_c \leq 0.5\, V$. Assuming that $M5$ and $M6$ are the same size, calculate the required $(W/L)$. Use the following parameters:

- $V_{T_{o,n}} = 0.7\, V$
- $V_{T_{o,p}} = -0.7\, V$
- $K_n' = 20\, \mu A/V^2$
- $K_p' = 10\, \mu A/V^2$
- $\gamma = 0.3\, V^{0.5}$
- $|2\Phi_F| = 0.6\, V$

Solution:

Assume that the cell will change state from 1 to 0, at $V_1$ falls below $V_{tn}$.

⇒ Initially

⇒ $M1$ (Cut off)
⇒ $M5$ (Sat.)

$V_{GS} = 0 - 5 = -5\, V$

$V_{DS} = 0.7 - 5 = -4.3\, V$

⇒ $M3$ (Lin.)
$V_{GS} = 5 - 0.5 = 4.5 \, V$

$V_{DS} = 0.7 - 0.5 = 0.2 \, V$

$I_{D,M5} = I_{D,M3}$

$$\frac{10}{2} \left( \frac{W}{L} \right)_{M5} (-5 + 0.7)^2 = 20 \left( \frac{2}{4} \right) \left[ (4.5 - 0.7)0.2 - \frac{1}{2} \times 0.2^2 \right]$$

$$\left( \frac{W}{L} \right)_{M5} = 0.08 = \left( \frac{W}{L} \right)_{M6}$$

Prob.3: Draw a 3T-DRAM cell and show its read and write operations.

Solution:

*Solved in lecture 10.*

References: