Bar Code

Digital Logic Design
(ELCT 201)

Spring 2009

Final Exam

Please read carefully before proceeding

a) The duration of the exam is **3 hours**.
b) Calculators are permitted for this exam.
c) Write your solutions in the space provided. If you need more space, write on the back of sheet containing the problem.
d) Attempt as much of the problems as you can within the time limits. The more you solve the higher your score is expected to be.
e) This exam booklet contains **12** pages, including this one.
f) Two extra sheets have been added at the end of the pages

Please do not write anything below

<table>
<thead>
<tr>
<th>Problem</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>maximum Marks</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>obtained Marks</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Problem no. 1

a) Design a combinational logic circuit 10:4 encoder which has a 10-bit input (D9 to D0) and a 4-bit output. If bit position i of input is 1 and all the other bit positions are 0, then the output will be i+2. For example, if the input (D9 to D0) is 0010000000, then the output will be 1010. (Note that D9 has the highest priority and D0 has the lowest priority).
Problem no. 2
A sequential circuit has two JK flip-flops A and B and one input x. The circuit is described by the following flip-flop input equations:

\[ J_A = Ax \quad K_A = B' \]
\[ J_B = B \times x \quad K_B = A \]

a) Derive the state equation \( A(t+1) \) and \( B(t+1) \).  \hspace{1cm} (5 marks)

b) Draw the state diagram of the circuit.  \hspace{1cm} (3 marks)
c) Show what’s the difference between Latch and Flip-flop  

(2 marks)

d) Draw state diagram of an elevator controller for a building with 25 floors. The controller has two inputs: UP and DOWN. It produces an output indicating the floor that the elevator is on. There is no floor 13, which is still a common architecture design technique.  

(5 Marks)
e) Design a circuit using D flip-flop for the state diagram in part (d). (10 Marks)
**Problem No. 3**
You are an engineer working for NASA. They want you to design a FSM that will test their newest rover Fido on the MIT campus. NASA wirelessly transmits the travel plans to Fido, and then Fido moves according to that information.

To design your FSM, you first select the following locations around the MIT campus and assign each location with a state in 3-bit binary representation: Killian[000], Kresge[001], ZCenter[010], Syd-Pac[011], Student Center[100], Building 34[101], 6.111 Lab[110], and the StataCenter[111].

To simplify your test, you inform NASA to send Fido’s FSM a binary sequence for travel plans (e.g. ‘1-0-0-0-1’ to cause Fido to move five times). In other words, Fido receives either ‘0’ or ‘1’ for each move and travels to the next destination as specified below. Fido starts off at Killian Court for each test run, and your FSM should output Fido’s current location.

- **Killian [000]:** If 0, stay at Killian. If 1, go to Kresge.
- **Kresge [001]:** If 0, go to Z-Center. If 1, go to Student Center.
- **Z-Center [010]:** If 0, go to Syd-Pac. If 1, go to Student Center.
- **Syd-Pac [011]:** If 0, stay at Syd-Pac. If 1, go to Killian.
- **Student Center [100]:** If 0, go to Stata Center. If 1, go to Building 34.
- **Building 34 [101]:** If 0, go to Syd-Pac. If 1, go to 6.111 Lab.
- **6.111 Lab [110]:** If 0, go to Stata Center. If 1, stay at 6.111 Lab.
- **Stata Center [111]:** If 0, go to Kresge. If 1, go to Building 34.

(a) Draw the state transition diagram for this FSM. Please use the back of an exam page for scratch space and make a neat copy of your final diagram below.  

(10 marks)

b) If Fido is forever given a sequence of ones (i.e. 11111…), where will it eventually end up?  

(3 marks)

c) If Fido is forever given a sequence of 01s (i.e. 010101…), which location(s) will it never visit?  

(3 marks)
d) Design a Circuit for the FSM in part (a) (note that the block diagram for Fido is given below) (9 marks)
In many communication and networking systems, the signal transmitted on the communication line uses a non-return-to-zero (NRZ) format. USB uses a specific version referred to as non-return-to-zero inverted (NRZI). A circuit that converts any message sequence of 0’s and 1’s to a sequence in the NRZI format is to be designed. The mapping for such a circuit is as follows:

(a) If the input message bit is a 0, then the output NRZI message contains an immediate change from 1 to 0, or 0 to 1, depending on the current NRZI value.

(b) If the input message bit is a 1, then the output NRZI message remains fixed at 0 or 1, depending on the current NRZI value.

For example, input Message: 10001110011010
Output NRZI message: 10100001000110

The input and output are serials.

a) Draw the FSM state diagram for the circuit. (5 marks)
b) Implement it using D Flip-flops and logic gates. \( (10 \text{ marks}) \)
c) Draw a state diagram for a recognizer that recognizes an input sequence 101001. It has an input X and output Y. The recognizer sets the output to 1 \( (Y = 1) \) for exactly one clock cycle if the last five values on the input X were 101001. \( (5 \text{ marks}) \)

d) Design the circuit for the above state diagram using T Flip-flop. \( (10 \text{ marks}) \)
Problem No. 5
Design a 4 bit up-down counter with parallel load using the following control inputs:

- The counter has three control inputs for the three operations: up, down, and load

(10 marks)
b) Design a 4-bit register with 2 control inputs $s1$ and $s0$, 4 data external inputs $I3$, $I2$, $I1$, $I0$, and 4 data outputs $Q3$, $Q2$, $Q1$, $Q0$. If $s1s0 = 00$, it means maintain the present value, $s1s0 = 01$ means load, and $s1s0 = 10$ means if external input $(I3I2I1I0) < (Q3Q2Q1Q0)$ maintain the same value (no change) else load external input. $s1s0 = 11$ means to rotate right by 1 bit, so 0101 would become 1010 and 1000 would become 0100.  

(10 marks)