I. INTRODUCTION

HIGH-FREQUENCY filters with wide programmability are important in several signal chains like hard-drive/CD/DVD electronics, where they are used for antialiasing and partial channel equalization. They are also relevant in multistandard radios (see, for example, [1]). The opamp RC architecture is attractive in such applications—the excellent linearity and low excess noise of active RC integrators can result in filters that consume very low power for a given dynamic range. However, designing high-frequency opamp RC filters is problematic, since the gain-bandwidth product of the opamps in an active RC biquad must be much larger than twice the \( f_o Q \) product of the highest quality pole pair of the filter transfer function. Moreover, the low-output-impedance stage required for the opamp is power hungry and has swing limitations. These problems can be avoided by replacing the opamp by an operational transconductance amplifier (OTA) with a sufficiently large transconductance [2]. Even so, the active RC architecture is (mostly) avoided at high frequencies due to the difficulties associated with the design of OTAs with adequate gain and bandwidth in low-voltage CMOS processes.

To address these issues, a power-efficient active RC integrator using a feedforward-compensated OTA was proposed in [3]. The tunable integrator and the single-ended block diagram of the OTA used in that work are shown in Fig. 1(a) and (b). The unity gain frequency of the integrator is programmed by using a resistor array. In the OTA, transconductors \( g_{m1} \) and \( g_{m2} \) are cascaded to achieve high dc gain. \( g_{m3} \) is a feedforward transconductor, which introduces a left-half-plane zero. When compared to a two-stage design, this structure is advantageous due to the following. The Miller capacitor required for compensation in a two-stage design needs to be charged and discharged at high frequencies, thereby necessitating significant bias current in the second stage. Since this is avoided in the feedforward-compensated structure, it is fundamentally more power efficient. This is borne out by the experimental results presented in [3]—where the authors report a filter with a maximum bandwidth of 350 MHz, consuming only 14 mA from a 1.8-V supply and achieving a dynamic range of 52 dB. The same authors present a 500-MHz antialias filter in [4], where a three-stage feedforward-compensated OTA is used. Several authors have since used feedforward-compensated opamps in active RC filters (see, for example, [5]). Feedforward compensation of opamps is not a new technique—several authors [6]–[8] make the observation that high dc gain and good phase margin can be obtained with such structures even in low-voltage CMOS processes.

While the results achieved in [3] and [4] are impressive, observing the measured results reveals that the shape of the frequency response varies significantly as the bandwidth setting is changed. Recall that the filter bandwidth is programmed by varying the integrating resistors, while keeping the OTA unchanged. This tuning strategy is problematic due to the following. At low-filter-bandwidth settings, the excess phase lag introduced by the nonidealities in the OTA is small, resulting in a filter response close to the desired response. When the bandwidth setting is increased, the excess phase increases. This results in \( Q \) enhancement in the filter and a peaking in frequency response at the band edge. One solution to this problem is to
design an OTA with so large a bandwidth that the integrator excess phase remains very small for all bandwidth settings. Designing such wideband OTAs would lead to significant power dissipation.

It is thus seen that the usual strategy of scaling only the integrating resistors while keeping the OTA unchanged results in a filter response whose shape varies with the bandwidth setting as seen in several reported works [3], [4], [9]. The problems associated with bandwidth programmability occur in all filter architectures. In the specific case of transconductance–capacitance filters, the use of constant- $C$-scaled integrators [10] mitigates this problem. In [11], the authors address the problem in baseband active RC filters. The strategy they adopt is to appropriately vary the gain-bandwidth product of the Miller compensated opamp as the bandwidth is programmed. This is accomplished by using a compensating capacitor array in the place of a fixed capacitor and a programmable first stage, thereby rendering the excess phase shift caused by the opamp independent of the bandwidth setting. While this might be sufficient for low-frequency filters, the use of switches in the signal path and scaling-only-selected transconductors does not seem to be an effective technique when the filter bandwidths are in the range of several hundreds of megahertz.

In this paper, we present an active RC technique that enables the design of high-frequency filters while maintaining frequency-response shape when the bandwidth is programmed over a wide range. The basic idea is to use the “constant-capacitance scaling” principle, hitherto applied to high-speed Gm- $C$ filters, in active RC filters. The rest of this paper is organized as follows. Section II describes constant- $C$-scaled active RC integrators. These integrators employ constant- $C$-scaled feedforward-compensated OTAs. A fifth-order singly terminated Chebyshev active RC ladder filter is used as a vehicle to demonstrate the efficacy of the proposed techniques. Implemented in a 0.18-$\mu$m CMOS process, the 3-dB bandwidth of the filter is digitally programmable from 44 to 300 MHz [12]. The test chip incorporates a resistor servo loop, an efficient bias-distribution technique, and provisions for accurate testing of the packaged prototype. The design of the filter and the supporting circuitry is discussed in Section III. Experimental results of prototype chips are shown in Section IV. As expected, the shape of the frequency response is maintained over the $7 \times$ programming range. At the highest bandwidth setting, the filter core achieves a dynamic range of 56.6 dB, while consuming 54 mW from a 1.8-V supply. Conclusions are given in Section V.

II. CONSTANT- $C$-SCALED ACTIVE RC INTEGRATORS

To preserve the shape of the frequency response of a linear network when the bandwidth is programmed, it is necessary to scale all the poles and zeros of the network by the same factor. One way of ensuring this in a network of transconductors is constant-capacitance scaling—where all conductances/transconductances in a network are multiplied by a factor $\alpha$, while all capacitances (both intentional and parasitic) remain unchanged. It can also be shown [13] that the integrated output noise of the network (considering thermal noise) and maximum signal-handling capability of the network (when it is nonlinear) are preserved under constant-$C$ scaling.

The block diagram of the programmable OTA used in this paper is shown in Fig. 2(a). $R_{\text{int}}$ and $R_{\text{e}}$ are the digitally programmable integrating resistor and feedforward-compensating resistor, respectively. The OTA is constant-$C$ scaled and based on the topology of Fig. 1(b). All the (trans)conductances in the OTA, $R_{\text{int}}$ and $R_{\text{e}}$, are digitally programmed by a 3-bit word $(b_0 \sim b_2)$.

A. Programmable OTA

The constant-$C$-scaled programmable active RC integrator proposed in this paper is shown in Fig. 2(a). $R_{\text{int}}$ and $R_{\text{e}}$ are the digitally programmable integrating resistor and feedforward-compensating resistor, respectively. The OTA is constant-$C$ scaled and based on the topology of Fig. 1(b). All the (trans)conductances in the OTA, $R_{\text{int}}$ and $R_{\text{e}}$, are digitally programmed by a 3-bit word $(b_0 \sim b_2)$. The schematic of the
unit transconductor is shown in Fig. 3(a). M1–M2 forms the main differential pair, the tail current of which is formed by M5–M6. The differential pair is turned on/off by switching the tail currents using triode-operated MOSFETs M3–M4. M9–M10 forms the pMOS load and are switched on/off using triode-operated MOSFETs M1–M2. Transistors M3–M4 form the dummy differential pair with M7–M8 as tail-current sources and M5–M6 as switches. When the main pair is “on,” the dummy pair is “off,” and vice versa. It can be shown that connecting many such unit transconductors in parallel results in a network where all nodal capacitances remain independent of the number of unit transconductors that are “on,” while all (trans)conductances scale in proportion to the number of active elements [10]. The tail currents of the differential pairs in the OTA are derived from a fixed-transconductance-bias circuit to keep the transconductance of the differential pair intact over process and temperature. The transconductance of each programmable transconductor cell in the OTA at the maximum bandwidth setting is 7 mS.

B. Programmable $R_{\text{int}}$

The programmable integrating resistor is realized by connecting binary-weighted unit resistances in parallel. The unit resistance used for this purpose can be realized in several ways as shown in Table I. We denote the resistance of the MOSFET and the unit resistor by $R_M$ and $R_{\text{unit}}$, respectively. $b$ is the control bit and takes on values of zero or one. Part (a) in the table shows a switch in series with a fixed polysilicon resistor. The switch is made large, so that $R_M/R_{\text{unit}} \ll 1$. Although this strategy has good linearity, the large parasitic capacitances associated with the switch are problematic in high-frequency filters. There is also no control over the integrating resistor across process and temperature.

An alternative approach is to use a MOSFET, operated in triode region (part (b) of Table I). A tuning loop is used to control the conductance of the MOSFET. The parasitics of the MOSFET are not a problem, as a small device is sufficient to realize the desired resistance. However, it suffers from poor linearity when compared to a polysilicon resistor.

Part (c) in Table I combines the merits of parts (a) and (b) and is used in this paper. Here, the resistance is realized as a series combination of a triode-operated MOSFET resistance and a fixed resistor. The resistance of the MOSFET is made a small percentage of the total resistance. This reduces the signal swing across the MOSFET, increasing the linearity. $R_{\text{unit}}$ can be kept constant across process and temperature by tuning the MOSFET resistance. In our design, the MOSFET contributes about 15% of $R_{\text{unit}}$. A servo loop controls the resistance of the transistor, so that $R_{\text{int}}$ is relatively constant over process and temperature. To reduce the size of the transistor, its gate is boosted above the supply voltage.

Fig. 4 shows the complete 3-bit programmable integrating resistor. The resistance of the array is controlled using logic signals $b0 \rightarrow b2$. The “switch-end” of the array is connected to the OTA virtual ground. Dummy resistors and switches are used in an attempt to keep the capacitance at the virtual-ground node the same, irrespective of the bandwidth setting. $M_{\text{d1}}$, $M_{\text{d2}}$, and $M_{\text{d3}}$ are the dummies corresponding to $M_0$, $M_1$, and $M_2$, respectively. Simulations show that maintaining the capacitance constant at the OTA virtual ground is critical. At the highest bandwidth setting, $R_{\text{int}}$ is 1.67 kΩ.

C. Programmable $R_z$

The programmable resistor $R_z$ compensates for the excess phase of the integrator caused by the feedforward effect of the integrating capacitor. It is realized using a bank of three binary-weighted MOS transistors operated in the triode region, as shown in Fig. 5. Since $R_z$ is small when compared to the impedance of the integrating capacitor in the frequency band of interest, the swing across it is small, and distortion is not an issue. Dummy transistors are used to maintain constant-C scaling. A tuning loop is used to stabilize $R_z$ over process and temperature variations.

Fig. 6 shows the benefits of constant-C scaling in a fifth-order Chebyshev ladder filter as its bandwidth is programmed over a 7× range. The details of the filter implementation are discussed in the next section. The responses in the figure are from transistor-level simulations. Fig. 6(a) shows the simulated responses when only the resistors are programmed to vary the bandwidth, with the OTA bandwidth fixed to the highest value (the usual
OTA. The pMOS loads use devices with twice the minimum length. The tail currents of all the transconductors are derived from a “fixed-transconductance-bias” generator. The details of the fixed-$g_m$-bias circuit and the bias-distribution technique are described later in this section.

### B. CMFB Circuit

The output common-mode voltage of each stage of the OTA is fixed by a separate common-mode feedback (CMFB) loop. Fig. 8 shows the CMFB circuitry. A resistive common-mode detector is used for linearity. The sensing resistors $R_{cm}$ are very large (220 kΩ) in relation to the integrating resistors. Such large-valued resistors can be realized, owing to the 1 kΩ/square polysilicon layer available in the process. Feedforward capacitors $C_{cm}$ (30 fF) are used to avoid the degradation of the loop phase margin due to the distributed capacitance of the transistors. The detected common-mode level is compared with a reference voltage, and the resulting error is amplified using an error amplifier formed by M1–M4. The source follower (M7) and $C_c$ (2 pF) form the compensating network for the CMFB loop. The two CMFB circuits required per OTA consume about 2 mA.

### C. Resistor Servo Circuit

To achieve good linearity and smaller device parasitics, the triode-operated MOS transistors in the integrating and feedforward-compensating resistor arrays (denoted by $R_t$ and $R_z$, respectively) are biased with gate voltages above the power supply. A resistor servo loop adjusts the value of the gate voltages so that $R_t$ and $R_z$ track an external resistor. The simplified schematic of the servo loop is shown in Fig. 9. $V_{sat}$ is a battery that boosts the control voltage above the supply. It is seen that, if the opamps are ideal, $R_t = R_{ext}/\alpha$ and $R_z = R_{ext}/\beta$. The voltage drop across $R_{sat}$ was chosen to be 200 mV. The battery is implemented by a large capacitor (2 pF) charged to an appropriate voltage ($V_{dd} + V_{th}$), as shown in Fig. 10.

### D. Fixed-Transconductance-Bias Generation

A fixed-transconductance-bias generator that is robust with respect to supply voltage and ambient temperature is used to stabilize the transconductances of the opamp over process and temperature. Fig. 11 shows the fixed-transconductance-bias generator employed in this design [14]. The salient features of this bias generator are the following.

1) The generator does not rely on the MOSFET square law, unlike more traditional circuits [15], [16].
2) The generated bias current is very tolerant of the large output conductances of short-channel MOSFETs.
3) The circuit is robust with power-supply variations.

Referring to Fig. 11, M1 and M2 are devices whose transconductance $g_m$ need to be stabilized. The circuit servos the $g_m$ of M1 and M2 to the stable off-chip conductance $1/R$. Circuit operation can be understood as a negative-feedback system. Any deviation of $g_m$, $M1$ from $1/R$ causes the negative feedback to adjust the current through M11 to bring $g_m$, $M1$ back to $1/R$. The drain potentials of M1 and M2 are identical and independent of the supply voltage. Simulations (in the absence of mismatch) show that $g_m$’s of M1 and M2 vary by less than 0.1%
for a Vdd varying between 1.6 and 2.0 V. M11’s drain–current is distributed to all transconductors on the chip.

**E. Bias-Distribution System**

The current generated by the fixed-Gm bias circuit should be mirrored to all the filter transconductors as accurately as possible. Fig. 12(a) shows the simplest circuit that can be used to do this. \( I_{\text{bias}} \) is generated in the fixed-Gm bias block and routed to the filter transconductor, where it is converted into a voltage by M2r. M2 represents the tail-current source of the filter transconductor (the switch used to turn the current source off is not shown for simplicity). Notice that the drain-source voltage of M2 is dependent on \( V_{\text{CM}} \), the input common-mode voltage of the filter. During chip layout, M2r and M2 should be placed in close proximity, which is easy to accomplish. One problem with this approach is that the current in M2 no longer equals \( I_{\text{bias}} \) due to the different drain-source voltages of M2r and M2. The drain current of M2 is seen to be \( I_{D,M2} = \frac{(1 + \alpha V_{DS,M2})}{(1 + \alpha V_{GS,M2})} I_{\text{bias}} \).

To mitigate this problem, a common solution is to employ the precise current mirror shown in Fig. 12(b). M1r is sized so that it has the same current density as M1 in the filter. Hence, M2 and M2r have the same \( I_{\text{bias}} \), thereby ensuring that the transconductor current is \( I_{\text{bias}} \). \( C_c \) compensates the negative-feedback loop formed by M2r, M1r, M3, and M4. While this approach certainly eliminates systematic error in the drain–current of M2, it poses a layout problem due to the following—four devices (M1r, M2r, M3, and M4) need to be placed in close proximity to M1 and M2. \( C_c \) is also usually larger than these devices. Since
M1 is a part of the high-speed signal path of the filter, it is preferable that the layout be compact. It is therefore seen that, while the simple technique of Fig. 12(a) is advantageous with respect to layout, it has poor accuracy. On the other hand, the circuit in Fig. 12(b) results in an accurate reproduction of current, while resulting in a suboptimal layout.

The basic idea behind the technique that combines the advantages of both circuits discussed earlier, while avoiding their disadvantages, is the following. Precision of the circuit of Fig. 12(a) could be improved by deliberately modifying $I_{1\text{bias}}$ to $I_p$, where $I_p = ((1 + \lambda V GS_{M2r})/(1 + \lambda V DS_{M2}))I_{1\text{bias}}$. Since $I_p$ is a predistorted version of $I_{1\text{bias}}$, the percentage error in the drain current of M2 is seen to be zero. A circuit that generates $I_p$ is shown in Fig. 12(c). The devices shown in the box are global. They are laid out far away from the high-speed signal path. M3 and M2r have identical sizes. It is easy to see that $I_p = I_{1\text{bias}}((1 + \lambda V GS_{M2r})/(1 + \lambda V DS_{M2r}))$. $I_p$ is sensed by precision pMOS mirrors, and multiple copies of $I_p$ are routed to the individual transconductors. At the transconductor, $I_p$ is mirrored by M2s’ – M2, generating $I_{1\text{bias}}$ in M2. Notice that the layout near the transconductors (the high-speed signal path) is very simple and compact. In practice, M2s’ and M2 are merged into the same multifinger structure. While the proposed technique is discussed here in the context of continuous-time filters, it is generic and can be applied to a whole range of analog-circuit blocks. A BiCMOS mirror employing a similar principle was used in [17].

F. Filter Testing

Accurately measuring the frequency response of the filter is a challenge due to the following. Since the filter is not a stand-alone block but intended to be a part of a larger SoC, it is not designed to drive package and board parasitics. On-chip buffers, which are turned on only during test time are used to interface the filter with the external world. The test buffers, the package, and the PCB used for characterization have a frequency response which must be deembedded to determine the characteristics of the filter accurately.

A conventional technique for accurate measurement of on-chip active filters is that proposed in [18], as shown in Fig. 13(a). T1 and T2 are baluns that accomplish single ended to differential conversion so that the fully differential filter can be measured with single-ended test equipment. Two measurement paths are created within the filter—one is a direct
path that bypasses the filter, and the other is the filter path. Both these paths contain two nominally identical test buffers, TB1 and TB2. It can be shown that, in the absence of package feedthrough, the filter response is the ratio of the responses of the filter path and direct path.

In a recent work [19], it was shown that the measurement technique of [18] is accurate in the filter passband but is prone to error in the filter stopband. The poor stopband-measurement accuracy was attributed to direct feedthrough in the IC package. It was shown experimentally that a simple polarity-reversal-switch network added before the buffers [as shown in Fig. 13(b)] could be used to effectively cancel package feedthrough. However, this technique has a few issues. First, the measurement accuracy is still limited by mismatch between the external measurement paths through the output baluns. The test buffers were implemented as source-follower stages driving a differential pair. While the linearity of a differential pair was adequate to test a Gm-C filter, it is clear that a more linear buffer is needed to accurately measure the distortion of an active RC filter (whose inherent distortion is smaller).

In this paper, we propose an improvement over the test method proposed in [19]. The technique is shown in Fig. 13(c). The outputs of the two test buffers are shorted together so that the external signal paths for the direct and filter measurements remain identical. Only one of these buffers is “on” at any time—thus, either the direct path or the filter path can be activated. Note that the only difference between the direct path and the filter path is the filter itself—the external path (package and PCB) are common to both paths. To improve the linearity of the test buffer, a resistive attenuator is used. A polarity-reversal-switch network is placed between the attenuator and the differential pair following the attenuator. This is used to cancel the effect of package feedthrough, as discussed in [19].

Fig. 14 shows the simplified schematic of the test buffer. It has a two-stage design. The first stage is a source follower formed by M1, M2, and current sources $I_1$. The second stage is a transconductor formed by M3–M6 and current source $I_2$. The first-stage output is attenuated by a factor of eight using a resistor divider. This enhances the linearity of the following stage at the expense of gain. Having a linear test buffer is important as the DUT is an active RC filter (which is expected to be linear). The output of the resistor divider is connected to the second stage (which is a cascaded differential pair) through a set of polarity-reversal switches implemented using transistors Ms1–Ms4. The gain polarity of the buffer (+ or −) is controlled by the bit $b_1$. The control bit $b_0$ is used to power down the buffer. When $b_0$ is low, all the bias currents and the bias voltage for the cascode transistors M5–M6 are switched off. $Rd$ damps any potential common-mode oscillation of the cascode and the package inductance. Each test buffer consumes 15 mA and is only turned on at test time.

IV. MEASUREMENT RESULTS

The filter test chip was fabricated in a 0.18-μm CMOS process through the Europractice program. The die photograph and the top-level layout of the chip are shown in Fig. 15. The filter has an active area of 0.63 mm² and is mounted in a 44-pin JLCC package.

A. Frequency-Response Measurements

Fig. 16 shows the measured frequency response of the filter for all bandwidth settings. The passband details are shown in the inset. It is seen that, owing to constant-$C$ scaling, the shape of the response remains virtually unaltered in spite of being programmed over a 7× range.

Fig. 17 shows the normalized response of 15 chips on the same plot, at the highest and lowest (in the inset) bandwidth settings. Good repeatability is seen.

B. Noise Measurements

Fig. 18 shows the measured noise spectral density at the output of the filter for all bandwidth settings. To make accurate measurements in spite of the high-noise figure of the spectrum analyzer, the filter output is amplified by a low-noise amplifier before being fed into the spectrum analyzer. The technique described in [19] was used to account for the frequency-dependent gain of the measurement paths. The rms output noise is $860 \mu V_{\text{rms}}$ at the highest bandwidth setting and increases to $1.3 \text{ mV}_{\text{rms}}$ at the lowest bandwidth setting. The increase in
the integrated noise for lower bandwidths is due to $1/f$ noise. The charge-pump-based resistor servo loop introduces clock feedthrough into the filter. The inset in Fig. 18 shows a zoomed version of the filter-output noise spectral density (for the lowest bandwidth setting). The clock frequency used in the charge pump is 1 MHz.

C. Distortion Measurements

Owing to the use of active $RC$ integrators, the measured third-harmonic distortion of the filter is 1% for a peak-to-peak differential input as large as 2.2 V. For the distortion test, the test tone was applied at one-third the band-edge frequency (which corresponds to the worst case tone for distortion measurement). The dynamic range of the filter for 1% harmonic distortion was measured as 56.6 dB for the highest bandwidth setting.

A two-tone test was performed to determine the intermodulation performance of the filter. Fig. 19 shows the $IIP_3$ of the filter as a function of the average frequency of the two input tones. For this test, the filter was set to the lowest bandwidth (44 MHz). The lowest $IIP_3$ is 2.5-V rms (the filter is “most nonlinear”) and occurs (as expected) at the band edge, since all the opamp output swings are large when the input-frequency content is at the band edge.

Table II summarizes the measured results.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Filter type</th>
<th>$0.18\mu$m CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>5th order Chebyshev, Opamp-RC</td>
<td>1.8 V</td>
</tr>
<tr>
<td>3-dB bandwidth</td>
<td>44-300 MHz</td>
<td></td>
</tr>
<tr>
<td>Active chip area</td>
<td>0.63 mm$^2$</td>
<td></td>
</tr>
<tr>
<td>Power (filter core)</td>
<td>54 mW</td>
<td></td>
</tr>
<tr>
<td>Integrated output noise</td>
<td>869 $\mu$V rms</td>
<td></td>
</tr>
<tr>
<td>$IIP_3$ @ band-edge</td>
<td>2.5 V rms</td>
<td></td>
</tr>
</tbody>
</table>

Table II

Summary of Measurement Results

- Test tone at $f_{\text{in}} = \frac{f_{\text{bw}}}{3}$
- $V_{\text{in,pp}}$ differential for $\text{THD} \leq -40 \text{ dB}$
- Dynamic range for $\text{THD} = -40 \text{ dB}$

$V_{\text{in,pp}} = 2.2 \text{ V}$

Dynamic range = 56.6 dB
Table III compares this paper with recently reported high-frequency CMOS filters. The figure of merit (FOM) used for comparison is [2]

\[
\text{FOM} = \frac{P_{\text{diss}}}{pQ_{\text{max}} f_0 DR^2}
\]

where \(P_{\text{diss}}\) is the power dissipation, \(p\) is the number of filter poles, \(f_0\) is the filter cutoff frequency, \(Q_{\text{max}}\) is the maximum quality factor of the filter poles, and \(DR\) is the dynamic range. A lower FOM indicates a more power-efficient design. [3] is a design with a feedforward OTA design similar to that used in this paper. However, the shape of the response changes significantly as the bandwidth is programmed. [4] uses a three-stage feedforward opamp in a 500-MHz filter design. The power dissipation does not include contributions from the tuning or bias-distribution circuitry. Since the OTA is kept fixed as the bandwidth setting is varied, the shape of the response changes with bandwidth setting. [20]–[23] are Gm-C filter designs. [20] achieves a 500-MHz bandwidth with a sharp transition band in a 0.35-\(\mu\)m process. As expected, the power efficiency is not as good as that in the active RC case. It is seen that the filter presented in this paper compares favorably with others reported in the literature—particularly considering that the frequency-response shape is maintained over a 7\(\times\) range.

V. CONCLUSION

Design considerations for widely programmable active RC integrators were given. A constant-\(C\) programmable active RC integrator based on a feedforward OTA was proposed. This integrator has the same dc gain and excess phase at all bandwidth settings, resulting in a constant frequency-response shape as the bandwidth is programmed over a wide range. This integrator was used as a building block in a fifth-order Chebyshev low-pass filter with a 3-dB bandwidth programmable from 44 to 300 MHz. The theory is borne out by measured results from a test chip fabricated in a 0.18-\(\mu\)m CMOS process. At the highest bandwidth setting, the filter achieves a dynamic range of 56.6 dB while consuming 54 mW from a 1.8-V supply.

REFERENCES


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