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Very Large Scale Integration (VLSI)

Lecture 3

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Contents

- Wiring tracks
- Latch-up
- Circuit characterization & performance
  - Resistance estimation
  - Capacitance estimation
  - Inductance estimation
- Delay estimation
  - Simple RC model
  - Penfield-Rubenstein Model
- Delay minimization techniques
  - Transistor sizing
  - Distributed drivers
  - Large driver
- Wiring techniques
Circuit characterization & performance

- Resistance estimation
- Capacitance estimation
- Inductance estimation
Parastic Elements

- So far, we've concentrated on getting circuit elements that we want for digital design
  - Transistors
  - Wires
- Parasitics - occur whether we want them or not
  - Capacitors
  - Resistors
  - Transistors (bipolar and FET)
Resistance estimation

- Resistance of uniform slab can be given as,

\[ R = \frac{\rho}{t} \cdot \frac{l}{w} \text{ ohms} \]

Where \( \rho = \text{resistivity} \)
\( t = \text{thickness} \)
\( l = \text{conductor length} \)
\( w = \text{conductor width} \)

or,

\[ R = R_s \cdot \frac{l}{w} \text{ ohms} \]

\( R_s \) is the sheet resistance \( \Omega/\square \)
Resistance estimation (cont.)

- Resistance of certain layers

<table>
<thead>
<tr>
<th>Material</th>
<th>$R_s \ (\Omega/\square)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>metal</td>
<td>0.03</td>
</tr>
<tr>
<td>Poly</td>
<td>15$\rightarrow$100</td>
</tr>
<tr>
<td>Diffusion p</td>
<td>80</td>
</tr>
<tr>
<td>Diffusion n</td>
<td>35</td>
</tr>
<tr>
<td>Silicide</td>
<td>2$\rightarrow$4</td>
</tr>
<tr>
<td>N-well</td>
<td>1K$\rightarrow$5K</td>
</tr>
</tbody>
</table>
Resistance estimation

For MOSFET channel resistance

\[ R_{\text{channel}} = R_{\text{Sheet}} \left( \frac{L}{W} \right) \]

where \( R_{\text{sheet}} = \frac{1}{\mu C_{\text{OX}} (V_{gs} - V_t)} \)

For P and n channels

\[ R_{\text{sheet}} = 1000 - 30,000 \ \Omega/\square \]
Resistance estimation (cont.)

Resistance of non rectangular regions

- Ratio = \( \frac{2L}{L+2W_1} \)
- Ratio = \( \frac{W_1}{W_2} \)
- Ratio = \( \frac{L}{W} \)
- Ratio = \( \frac{W_2}{W_1} \)
Resistance

- Depends on resistivity of material $\rho$ (Rho)
- Sheet resistance $R_s = \frac{\rho}{t}$
- Resistance $R = R_s \times \frac{L}{W}$
- Corner approximation - count a corner as half a square

Example:
$R = R_{s(poly)} \times 13 + 2 \times \frac{1}{2} + 3 \times \frac{1}{2}$ squares
$R = 4\Omega/sq \times 15.5$ squares = $62\Omega$
Inverter resistance estimation

- CMOS inverter (no static current)
- Switching current

\[ I_{\text{max}} = \frac{V_{DD}}{R_{\text{total}}} = \frac{V_{DD}}{R_{s,p} \frac{L}{W} + R_{s,n} \frac{L}{W}} \]

for \( L = W = 1 \)

\[ I_{\text{max}} = \frac{V_{DD}}{R_{s,p} + R_{s,n}} = \frac{V_{DD}}{25 + 10} = \frac{V_{DD}}{35} \]

Switching power loss = \( I_{\text{max}} \cdot V_{DD} = \frac{V_{DD}^2}{35} \)
Circuit characterization & performance

- Resistance estimation
- Capacitance estimation
  - Transistor capacitance
  - Routing capacitance
- Inductance estimation
- Delay estimation
Capacitance estimation

The dynamic response of MOS systems strongly depends on the parasitic capacitances associated with the MOS device. The total load capacitance on the output of a CMOS gate is the sum of:

- gate capacitance (of other inputs connected to out)
- diffusion capacitance (of drain/source regions)
- routing capacitances (output to other inputs)
Capacitance (1/2)

- Transistors
  - Depends on area of transistor gate
  - Depends on physical materials, thickness of insulator
  - Given for a specific process as $C_g$
- Diffusion to substrate
  - **Side-wall capacitance** - capacitance from periphery
  - **bottom-wall capacitance** - capacitance to substrate
  - Given for a specific process as $C_{\text{diff,bot}}$, $C_{\text{diff,side}}$
Capacitance (2/2)

- Metal to substrate
  - Parallel plate capacitance is dominant
  - Need to account for fringing, too
- Poly to substrate
  - Parallel plate plus fringing, like metal
  - don’t confuse poly over substrate with gate capacitance
- Also important: capacitance between conductors
  - Metal1-Metal1
  - Metal1-Metal2
Capacitance estimation (cont.)

- Gate capacitance
- Diffusion capacitance
- Routing capacitance

- $C_{\text{diff}} > C_{\text{poly}} > C_{m1} > C_{m2}$
Capacitance estimation

- In general, capacitance could be calculated using

\[ C = \frac{\varepsilon \cdot A}{d} = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot A}{d} \]

\[ C_{/\text{unit area}} = \frac{\varepsilon_0 \cdot \varepsilon_r}{d} = C_{ox} \]
Gate Capacitance

\[ C_g = C_{gs} + C_{gd} + C_{gb} \]
Capacitance estimation (cont.)

- Diffusion capacitance (source/drain)

\[ C_{s, \text{diff}} = C_{d, \text{Area}} \cdot A + C_{d, \text{sidewalls}} \cdot p \]

Where \( A = \text{area} \) and \( p = \text{perimeters} \)
Routing capacitance

- single conductor capacitance
- multiple conductor capacitance
Capacitance estimation (cont.)

Routing capacitance: a) single conductor capacitance

\[
C_{total} = \varepsilon \left[ \frac{w - \frac{t}{2}}{h} + \frac{2\Pi}{\ln \left[ 1 + \frac{2h}{t} + \sqrt{\frac{2h}{t} \left( \frac{2h}{t} + 2 \right)} \right]} \right]
\]

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Routing capacitance: b) multiple conductor capacitance

\[ \Delta V_{out} = \Delta V_{in} \cdot \frac{C_{12}}{C_2 + C_{12}} \]
Multilayer capacitance calculations

Example: given the layout shown in the figure calculate the total capacitance at source and gate given that:

\[
\begin{align*}
C_{\text{metal/Area}} &= 0.025 \mu F/\mu m^2 \\
C_{\text{poly/Area}} &= 0.045 \mu F/\mu m^2 \\
C_{\text{Gate/A}} &= 0.7 \text{ fF}/\mu m^2 \\
C_{d,a/A} &= 0.33 \text{ fF}/\mu m^2 \\
C_{d,\text{side/L}} &= 2.6 \text{ fF}/\mu m \\
\lambda &= 5.1 \mu m
\end{align*}
\]
Solution

Source capacitance

\[ C_{S,\text{diff}} = C_{d,A} \cdot A + C_{d,\text{side walls}} \cdot P \]

\[ A = 4\lambda \cdot 3\lambda = 12\lambda^2 \]

\[ P = 2(4\lambda + 3\lambda) = 14\lambda \]

So, \( C_{S,\text{diff}} = 0.33 \cdot 12\lambda^2 + 2.6 \cdot 14\lambda = 63.51\text{fF} \)
Solution (cont.)

Gate capacitance

\[ C_{G,\text{total}} = C_M + C_{MP} + C_{P1} + C_G + C_{P2} \]

\[ C_M = 0.025 \times 100\lambda \times 3\lambda = 7.5\lambda^2 \]

\[ C_{MP} = 0.045 \times 4\lambda \times 4\lambda = 0.72\lambda^2 \]

\[ C_{P1} = 0.045 \times 2\lambda \times 2\lambda = 0.18\lambda^2 \]

\[ C_{P2} = 0.045 \times 2\lambda \times 2\lambda = 0.18\lambda^2 \]

\[ C_G = 0.7 \times 2\lambda \times 3\lambda = 4.2\lambda^2 \]
Example Problems - Parasitic Calculation (1/10)

\[ R_{metal1} = ? \quad R_{poly} = ? \quad R_{ndiff} = ? \]
\[ C_{metal1} = ? \quad C_{poly} = ? \quad C_{ndiff} = ? \]
Example Problems - Parasitic Calculation (2/10)

R_{metal1} = \left( \frac{30\lambda}{3\lambda} \right) \times 0.08\Omega/\square = 0.8\Omega

C_{metal1} = (30\lambda \times 0.25\mu m/\lambda) \times (3\lambda \times 0.25\mu m/\lambda) \times 0.04fF/\mu m^2 + (30\lambda + 3\lambda + 30\lambda + 3\lambda) \times 0.25\mu m/\lambda \times 0.09fF/\mu m
\quad = 0.225fF + 1.485fF
\quad = 1.71fF
Example Problems - Parasitic Calculation (3/10)

\[
\text{R_{ndiff}} = \left( \frac{11\lambda}{3\lambda} \right) \times \frac{2\Omega}{\Box} = 7.33\Omega
\]

\[
\text{C_{ndiff}} = \left( 11\lambda \times 0.25\mu m/\lambda \right) \times \left( 3\lambda \times 0.25\mu m/\lambda \right) \times 0.6fF/\mu m^2 + \left( 11\lambda + 3\lambda + 11\lambda + 3\lambda \right) \times 0.25\mu m/\lambda \times 0.2fF/\mu m
\]

\[
= 1.24fF + 1.4fF
\]

\[
= 2.64fF
\]
Example Problems - Parasitic Calculation (4/10)

\[ R_{\text{poly}} = \left( \frac{3\lambda}{2\lambda} + \frac{1}{2} \square + \frac{8\lambda}{2\lambda} \right) \times \frac{4\Omega}{\square} = 24\Omega \]

\[ C_{\text{poly}} = \left( \left( \frac{3\lambda \times 0.25\mu m}{\lambda} \right) \times \left( \frac{2\lambda \times 0.25\mu m}{\lambda} \right) \right) + \left( \left( \frac{10\lambda \times 0.25\mu m}{\lambda} \right) \times \left( \frac{2\lambda \times 0.25\mu m}{\lambda} \right) \right) \times 0.09fF/\mu m^2 + \left( \frac{5\lambda + 10\lambda + 2\lambda + 8\lambda + 3\lambda + 2\lambda}{\lambda} \right) \times 0.25\mu m/\lambda \times 0.04fF/\mu m \]
\[ = 0.15fF + 0.3fF \]
\[ = 0.45fF \]
Example Problems - Parasitic Calculation (5/10)

\[ R_{metal1} = 0.8 \Omega \]
\[ C_{metal1} = 1.71 \text{fF} \]
\[ R_{ndiff} = 7.33 \Omega \]
\[ C_{ndiff} = 2.64 \text{fF} \]
\[ R_{poly} = 24 \Omega \]
\[ C_{poly} = 0.45 \text{fF} \]
What are the parasitic capacitances visible from point “A”?

\[ \lambda = 0.25 \mu m \]

\[ A \]

\[ C_{\text{poly}} \quad C_{\text{gate}} \quad C_{\text{coverhang}} \]
What are the parasitic capacitances visible from point “A”?

\[
C_{\text{poly}} = (6\lambda \times 0.25\mu\text{m}/\lambda) \times (2\lambda \times 0.25\mu\text{m}/\lambda) \times 0.09\text{fF/}\mu\text{m}^2 + (6\lambda + 2\lambda + 6\lambda + 2\lambda) \times 0.25\mu\text{m}/\lambda \times 0.04\text{fF/}\mu\text{m}
\]

\[
= 0.675\text{fF} + 0.16\text{fF}
\]

\[
= 0.84\text{fF}
\]
What are the parasitic capacitances visible from point “A”?

\[ C_{\text{gate}} = (3\lambda \times 0.25\mu\text{m/}\lambda) \times (2\lambda \times 0.25\mu\text{m/}\lambda) \times 0.9\text{fF/\mu m}^2 \]

\[ = 0.34\text{fF} \]

Remember: use \( C_g \), not \( C_{\text{poly}} \) for transistor gates!
What are the parasitic capacitances visible from point “A”?

\[ C_{\text{overhang}} = (2\lambda \times 0.25\mu m/\lambda) \times (2\lambda \times 0.25\mu m/\lambda) \times 0.09fF/\mu m^2 + (2\lambda + 2\lambda + 2\lambda + 2\lambda) \times 0.25\mu m/\lambda \times 0.04fF/\mu m \]

\[ = 0.0225fF + 0.08fF \]

\[ = 0.1fF \]
What are the parasitic capacitances visible from point “A”?

\[ \lambda = 0.25 \mu m \]

A

- \( C_{\text{poly}} \): 0.84 fF
- \( C_{\text{gate}} \): 0.34 fF
- Coverhang: 0.1 fF

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Inductance estimation

- Inductance is normally small but as the process shrink on-chip inductance must be taken into account.
- Bond-wire inductance can cause deleterious effects in large, high speed I/O buffers.
- The inductance of bonding wires and the pins on packages could be calculated by,

\[
L = \frac{\mu}{2\pi} \ln \left( \frac{8h}{w} + \frac{4h}{d} \right)
\]

Design techniques to overcome this problem:
- separate power pins for I/O pads and chip core
- multiple power and ground pins
- careful selection of the position of the power and ground pins on the package
- adding decoupling capacitances on the board
- increase the rise and fall times
- use advanced package technologies (SMD, etc)