Microelectronics

Chapter 8:

CMOS Voltage to Current Converters
Or
CMOS Transconductance Amplifiers
Or
CMOS Operational Transconductors (OTA)
CMOS Transconductors

■ Objectives and outlines:

1. Introduction
2. Famous Types of Transconectors
3. CMOS Realizations of different types of Tran conductors:
   (a) Single Input Single Output Transconductor
       Using CMOS Composite Transistor
   (b) Differential Input-Single Output Transconuctor
   (c) Differential Input- Differential Output Transconuctor
   (d) Differential Input- balanced Output Transconuctor
4. $G_m$-C continuous time filters
1. Introduction: OTA Evolution

- Bipolar OTA is introduced by RCA (Radio Corporation of America)
- Programmable active filters and linear circuits using discrete bipolar OTA. Preliminary work on M-S tuning
- CMOS OTA-C Filter with on-chip tuning
- Active Filter Design using OTA: A tutorial
- Linearization Techniques
- Q-tuning & tuning enhancement, high-frequency pseudo Differential OTAs

Timeline:
- 1969
- 1971
- 1982
- 1985
- 1988
- 1993
- Present
1. Introduction: OTA Evolution

► The bipolar transconductance amplifier (OTA) was commercially introduced in 1969 by RCA.

► Designers began using OTAs in the middle 80’s, since then the CMOS-OTA has become a vital component in a number of electronic circuits, both in open loop and in closed loop applications.

► Continuous-time filters implemented with transconductance amplifiers and capacitors known as Gm-C or OTA-C are very popular for a host of applications.
A few examples of continuous-time filters in a host of applications:

(1) Read channel of disk drives (for phase equalization and smoothing the waveform)

Top view of a 36 GB, 10,000 RPM, IBM SCSI server hard disk, with its top cover removed.
LPF is needed to:
- Limit signal and noise bandwidth;
- Provide anti-aliasing prior to sampling;
- Provide significant contribution to overall equalization.
(2) Receivers and Transmitters in wireless applications
(Used in PLL (Phase Locked Loop) and for Channel selection and interference rejection)

Low-IF Bluetooth Receiver
2. Famous Types of Transconectors

- **Single Input-Single Output Transconuctor:**
  \[
  I_{out} = G_m \, V_{in}
  \]

- **Differential Input-Single Output Transconuctor:**
  \[
  I_{out} = G_m \, (V_1 - V_2)
  \]

Where \( G_m \) is the transconductance gain.
Differential Input- Differential Output Transconductor:

\[ I_{out1} - I_{out2} = G_m (V_1 - V_2) \]

Differential Input- Balanced Output Transconductor:

\[ I_{out1} = -I_{out2} = G_m (V_1 - V_2) \]

Where \( G_m \) is the transconductance gain
General Requirements:

1. High Input Impedance
   (Inputs are connected to the gates of the MOS transistors)

2. High Output Impedance

3. Linearity
   (Output Current is linear function of single/differential input voltage)

4. High Unity Gain Frequency

5. Linear Transconductance Dependence on Control Voltage Or Current.
a. Single Input Single Output Transconductor Using CMOS Composite Transistor:

1. What is CMOS Composite Transistor?

\[ I_D = \frac{K_1}{2} (V_{GS1} - V_{Tn})^2 \]

\[ V_{GS1} = V_{Tn} + \frac{1}{\sqrt{K_1}} \sqrt{2I_D} \]

\[ I_D = \frac{K_2}{2} (V_{SG2} - |V_{TP}|)^2 \]

\[ V_{SG2} = |V_{TP}| + \frac{1}{\sqrt{K_2}} \sqrt{2I_D} \]

\[ V_{GSeq} = V_{GS1} + V_{SG2} = V_{Tn} + |V_{TP}| + \left( \frac{1}{\sqrt{K_1}} + \frac{1}{\sqrt{K_2}} \right) \sqrt{2I_D} \]

M1 and M2 are assumed Sat.

\[ V_{Teq} = \frac{1}{\sqrt{K_{eq}}} \]
\[ V_{Teq} = V_{Tn} + |V_{TP}| \]

\[ K_{eq} = \sqrt{\frac{K_1 K_2}{K_1 + K_2}} \]
(a) Single Ended Composite Transistor Transconductor

The output current of shown transconductor is given by:

\[ I_{out} = I_2 - I_1 \]

Where \( I_1 \) and \( I_2 \) are the drain current of the composite transistors (M1&M2) and (M3&M4).

\[
I_1 = \frac{K_{1eq}}{2} (V_C - V_{in} - V_{Teq})^2
\]

\[
I_2 = \frac{K_{2eq}}{2} (V_{in} + V_C - V_{Teq})^2
\]

Assuming the two composite transistors are matched \( \Rightarrow K_{1eq} = K_{2eq} \)
\[ I_{out} = I_2 - I_1 = \frac{K_{eq}}{2} \left[ (V_{in} + V_C - V_{Teq})^2 - (V_C - V_{in} - V_{Teq})^2 \right] \]

\[ I_{out} = I_1 - I_2 = 2K_{eq} (V_C - V_{Teq}) V_{in} \]

Note That: The output current \( I_{out} \) is linear function of the input \( V_{in} \) signal voltage and the equivalent transconductance value is given by:

\[ G_m = 2K_{eq} (V_C - V_{Teq}) \]

And \( G_m \) is linearly controlled by the control voltage \( V_C \).
Performance Issues:

1. Threshold modulation due to bulk effect precludes strict linearity.
2. Threshold voltage and thus the effective transconductance is temperature dependent.
3. Matching of Composite transistors is imprecise.
4. Effective transconductance, $G_m$ is tunable via balanced control voltage applied to gate of $M_1$ and $M_4$.

\[
I_{out} = G_m V_{in}
\]

\[
G_m = 2K_{eq} (V_C - V_{Teq})
\]
Project(2-i): Using PSpice simulation and 0.25µm model, design the shown transconductor to realize equivalent transconductance of 100µA/V such that the linearity range of this transconductor is maximum as possible.

- **Required Simulations:**
  1. $I_{out}-V_{in}$ DC characteristic indicating the designed value of $V_C$ and the aspect ratios of the four MOS-Transistors assuming $V_{DD}=-V_{SS}=2.5$ V assuming the body effect is neglected.
  2. $I_{out}-V_{in}$ DC characteristic with $V_C$ tuned from 0.8 $V_C$ to 1.2 $V_C$ with step 0.2 $V_C$.
  3. Frequency response for $V_{in}=1$ V AC while driving a load of 20 pF. Find the break and unity gain frequency.
  4. Find the output impedance at equivalent transconductance of 100µA/V as a function of frequency.
  5. Repeat (1,2,3,4) taking into account the body effect.

\[ I_{out} = G_m V_{in} \]

\[ G_m = 2K_{eq} (V_C - V_{Teq}) \]
(b) Differential Input-Single Output Transconductor

Differential pair as a voltage to current converter (Transconductor)

Assumptions:
- All transistors operating in saturation region.
- Differential pair (M1-M2) are matched with transconductance parameter K.
- Current Mirror (M3-M4) are also matched with unity current gain.

\[ I_{out} = I_1 - I_2 = \sqrt{I_{ss}}KV_{id} \left( \sqrt{1 - \frac{V_{id}^2}{4I_{ss}/K}} \right) \]
Note that:

\[ I_{out} = I_1 - I_2 = \sqrt{I_{SS} K V_{id}} \left( \sqrt{1 - \frac{V_{id}^2}{4 I_{SS} / K}} \right) \]

Simulation Results of the differential pair transconductor using different aspect ratios of M1 and M2.

(WL)_{1,2} = 100
(WL)_{1,2} = 10
(WL)_{1,2} = 1

I_{SS} = 100 \mu A

Nonlinear term

Linearity range

K \uparrow \quad G_m \uparrow
How to improve the linearity of the differential pair transconductor?

There are many circuit techniques proposed in many research papers to enhance the linearity of the differential pair transconductor by reducing or cancelling the nonlinear term.

Example: The Differential pair with degeneration resistor
Project(2-ii): Journal Article Project

In this part, you will read selected article from the IEEE Transactions on Circuits and systems-II and write a short report. The article is:

A Linear MOS Transconductor Using Source Degeneration and Adaptive Biasing (IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING, VOL. 48, NO. 10, OCTOBER 2001)

Read the article, and write a short report with the following sections:

1. Affiliation. Where do the authors work? Which university or company do they work for?

2. The Problem. In 2-3 paragraphs, answer the question: What problem is the article addressing? For example, what limitation did previous circuits have that this circuit solves? For this part and the following parts, do not plagiarize from the paper! Use your own words to answer these questions. Do not copy sentences from the paper!

3. The Approach. In 2-4 paragraphs, what approach do the authors use to address the problem? Do they run a simulation, build a circuit, or develop a new analytical technique? Discuss the type of simulation, VLSI process, or models used.
Project(2-ii): Journal Article Project

4. Results. In 2-3 paragraphs, summarize the results of the paper. Do the authors measure quantitative figures of merit? What are they?

5. Previous Work. Have the authors of this paper done any related work in this area previously? Look through the list of citations (references) at the end of the article, and list any citations that include any of this article’s authors.

Note:

The report must be typed, not handwritten.
(c) Differential Input- Differential Output Transconductor

The basic structure of the fully differential transconductor

The output currents of the differential transconductor shown are given by:

\[ I_{\text{out1}} = I_{\text{bias}} - I_a \]

\[ I_{\text{out2}} = I_{\text{bias}} - I_b \]

\[ I_{\text{out1}} - I_{\text{out1}} = I_b - I_a \]
Example: Differential Input – Differential Output Transconductor based on four- MOS transistor cell

Assumptions:
• Transistors (M1 to M4) are operating in saturation region. And matched with transconuctance parameter K.

\[ I_{out1} - I_{out1} = I_b - I_a = (I_2 + I_4) - (I_1 + I_3) \]

\[ I_{out1} - I_{out1} = K(V_b - V_a)(V_1 - V_2) \]

\[ G_m = K(V_b - V_a) \]
Simulation Results:

1. PSpice simulations were carried out with transistors aspect ratios \((W/L)_{1,\ldots,4} = 4\) and supply voltage of 2.5V.
2. The I-V characteristics with control voltage \(V_{ba} = 0.45\) V, \(V_1\) and \(V_2\) scanned from -1.25 V to 1.25 V.
Simulation Results:

- PSpice simulations were carried out with transistors aspect ratios $(W/L)_{1,...,4} = 4$ and supply voltage of 2.5V.
- The magnitude and phase frequency response

Note that the 3-dB point at more than 100 MHz

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(d) Differential Input- Balanced Output Transconductor

The basic structure of the balanced output transconductor

\[
\begin{align*}
\text{Voltage to current converter} \\
I_{\text{out}} &= (I_b - I_a) \\
I_a &= I_b \\
V_{\text{pp}} &= \text{Supply voltage} \\
V_{\text{ss}} &= \text{Ground}
\end{align*}
\]
Example: Differential Input – Balanced Output Transconductor based on four-MOS transistor cell

Assumptions:
- Transistors (M1 to M4) are operating in saturation region. And matched with transconductance parameter $K$.
- All current mirrors are matched.

\[
I_{out1} = -I_{out2} = I_a - I_b = (I_1 + I_3) - (I_2 + I_4)
\]

\[
I_{out1} - I_{out1} = K(V_a - V_b)(V_1 - V_2) \quad \rightarrow \quad G_m = K(V_a - V_b)
\]