Integrated Circuits Design (ELCT 701)

Final Exam

Please read carefully before proceeding.
1. The duration of this exam is 3 hours
2. Solve as much as you can
3. Only calculators are permitted for this exam
4. This exam booklet contains 12 pages including this one.

<table>
<thead>
<tr>
<th>Problem Number</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Possible Marks</td>
<td>40</td>
<td>30</td>
<td>30</td>
<td>15</td>
<td>115</td>
</tr>
<tr>
<td>Final Marks</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Prob. 1 (40 points) Consider a CMOS inverter, with the following parameters:

- nMOS: \( V_{To,n} = 0.8V \)  \( \mu_nC_{OX} = 50 \mu A/V^2 \)
- pMOS: \( V_{To,p} = -1.0V \)  \( \mu_pC_{OX} = 20 \mu A/V^2 \)

The power supply voltage \( V_{DD} = 5V \). Both transistors have a channel length of \( L_n = L_p = 1\mu m \) and the output load capacitance is 2pF.

(a) Determine the channel width of the nMOS and the pMOS transistors such that the switching threshold voltage is equal to 2.2V and the output rise time is \( \tau_{rise} = 5ns \).

(b) Calculate the average propagation delay time \( \tau_p \) for the circuit designed in (a).

(c) Calculate the dynamic power dissipation.

(d) If we want to re-design the inverter so that the propagation delay times are reduced by 25%. Determine the required channel dimensions of the nMOS and pMOS transistors. How does this re-design influence the switching threshold voltage \( V_{th} \)?
Prob. 2 (30 points) Given that the inputs are available on a clock cycle and the output is expected to appear in the following clock cycle, implement the following logic function:

\[ X = ((A.B.G) + C.(D + E)).(F.H + I) \]

Using Dynamic Transmission Gate, Domino, NORA and TSPC
i) Show the circuit on the transistor level.
ii) Assuming all minimum size transistors and only positive signals are available as inputs (inverters should be considered), compare between different implementations from area point of view (note: number of transistors).
iii) Explain the possibility of charge sharing problems in your implementations and suggest a method to overcome it.
**Prob. 3 (30 points)** for the following logic function

\[ X = (A.B.M.F + C.(D + E)).(G.H + I) \]

Implement the logic function using

i) CMOS and size the transistors to have the worst case output resistance as 1\(\mu\)m/1\(\mu\)m NMOS, 2.5\(\mu\)m/1\(\mu\)m PMOS inverter

ii) Transmission Gate,

For each family, show the circuit on the transistor level. Compare between different implementations from number of transistors.
Prob. 4 (15 points) consider the SRAM cell shown in the figure. Transistors M1 and M2 have (W/L) values of 4/4. Transistors M3 and M4 have (W/L) values of 2/4. M5 and M6 are to be sized such that the state of the cell can be changed for $V_c=0.5\text{V}$. Assuming that M5 and M6 are the same size, calculate the required (W/L). The supply voltage $V_{DD}=5\text{V}$ and use the following parameters:

$V_{T0,n} = 0.7\text{V}$

$V_{T0,p} = -0.7\text{V}$

$K_{n}^*=20\text{uA/\text{V}^2}$

$K_{p}^*=10\text{uA/\text{V}^2}$

$\gamma = 0.4\text{ V}^{1/2}$

$|2\varphi_F|=0.6\text{ V}$